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REMARKS

Claims 7-8 have been canceled. Claims 1-6 remain pending in the application.

Applicants amend claims 1 and 2 for clarification. No new matter has been added.

Applicants respectfully request that the Examiner indicate acceptance of the drawings.

Claim 2 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

Applicants amend claim 2 to clearly recite the feature of storing the input signal "sequentially to the first memory part, the second memory part, and the third memory part." Accordingly, Applicants respectfully request that the Examiner withdraw the § 112, ¶ 2 rejection.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,151,334 to Kim et al.; claims 3-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,504,855 to Matsunaga; claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,874,048 to Knapp et al.; and claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,721,295 to Brown. Applicants amend claims 1-2 in a good faith effort to clarify the invention as distinguished from the cited references, and respectfully traverse the rejection.

The Examiner relied upon the description in Kim et al. of an embedding unit 22 and a removing unit 24 as alleged disclosure of the claimed invention. The Examiner further contended that the claimed invention reads on a de-multiplexor. Applicants respectfully submit that a de-multiplexor does not include the features recited in the claims, as highlighted below. Indeed, the Examiner relied upon the description of de-multiplexor 74 in removing unit 24 of

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Kim et al. as alleged disclosure of the claimed extracting part. Kim et al. only describe, however, multiplexor 48 sending a signal to the removing unit 24, and do not disclose the multiplexor 48 receiving any signal from the removing unit 24.

In other words, Kim et al., as relied upon by the Examiner, fail to disclose,

“ device for processing data signals, comprising:
a plurality of input interfaces each inputting an input signal;
and
a multiplexing circuit multiplexing a plurality of output signals from the plurality of input interfaces,
wherein said each of the plurality of input interfaces comprises:
a storing part storing the input signal; and
an extracting part extracting said data signals included in said input signal from said storing part and outputting said data signals to said multiplexing circuit,
wherein said extracting part receives storage state information of said input signal from said storing part and outputs said data signals based on the storage state information,” as recited in claim 1. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 1 is patentable over Kim et al. for at least the above-stated reasons. The Examiner relied upon the additional references to specifically address the features recited in the dependent claims. As such, the additions of these references would still have failed to cure the aforementioned deficiencies of Kim et al. even assuming, arguendo, that such additions would have been obvious to one skilled in the art at the time the claimed invention was made. Accordingly, Applicants respectfully submit that claims 2-6 are patentable over the cited references, separately and in combination, for at least the foregoing reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider

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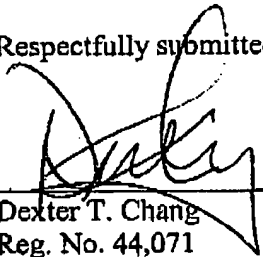
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this application not to be in condition for allowance, the Examiner is respectfully requested to

telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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